Very Large Scale Integration (VLSI) Systems, IEEE Transactions on (Volume:19 , Issue: 9)

Efficient Design of a Hybrid Adder Using Quantum-Dot Cellular Automata

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February 2012

***Abstract*---** *The saying goes that if you can count, you can control. Addition is a fundamental operation for any digital system, digital signal processing or a control system. A fast and accurate operation of a digital system is greatly influenced by the performance of resident adders. In this regard, an efficient hybrid adder that combines a carry select adder and a ripple carry adder using QCA technology is designed to meet all the needs that is indispensable for a digital circuitry. QCA is an emerging nanotechnology, with the potential for higher speed, smaller size, and lower power consumption than transistor-based technology. Recent development in nano electronics provides a good introduction to the quantum mechanics of electrons, notions of free and confined electrons. Hence, with the help of QCA technology, the proposed hybrid adder produces a lesser area-delay product when compared to the previous adders and this proposed adder is also applied to a Wallace tree multiplier, here the area-delay product is reduced and speed of the multiplier is augmented.*

***Keywords*---** *Hybrid Adder, QCA-Quantum-Dot Cellular Automat, Nano Electronics*

I. INTRODUCTION

VARIOUS nano electronic devices have been of interest to the research community during the last decade. These include carbon nanotubes, silicon nanowires, resonant tunneling diodes, and others. These devices have emerged as alternatives to the traditional VLSI technology based on CMOS. Conventional device physics is based on a free electron model and as device dimensions shrink, this model is not appropriate since the energies an electron is allowed to have become discrete. Recent book on nanoelectronics provides a good introduction to the quantum mechanics of electrons, notions of free and confined electrons as well as single electron and many electron devices. One of the devices suggested in the literature as an alternative to the traditional CMOS-based technology is the quantum-dot cellular automata (QCA). In QCA, the device used for logic is also used for interconnect. The basic logic gates in the QCA architecture are the majority gate (also referred to as the majority voter) and the inverter. The focus of the proposed work is on design of arithmetic circuits in QCA. One possible approach is based on examination of the best adders (meeting some criteria) developed for existing technologies such as CMOS for adaptation to new ones such as QCA. The following two directions are considered in this proposed work i.e. area occupied by basic logic elements in a QCA design and examining optimization of logic. The "quantity" of logic also indirectly determines the "amount" of QCA wires in a design. Addition is one of the fundamental arithmetic operations. A number of fast adder architectures have been proposed in the long history of computer arithmetic in pursuit of three basic characteristics: a regular structure, a fast logic evaluation and a compact circuit layout. Hybrid adders combine elements of different approaches to obtain adders with a higher performance, reduced area and low power consumption. Thus, with the help of QCA technology a hybrid adder that combines carry select adder and ripple carry adder is designed which reduces the area-delay product of the adder.

II. RELATED WORKS

Prior work on adder designs has examined a few directions. Wang [3] present an efficient design of a 1-bit QCA adder that uses three majority gates and two inverters. Majority logic reduction for several three variable Boolean functions is studied in [4]. A performance comparison of some QCA adder is presented in [5]. Modular design of conditional sum adders is studied in [6]. Tang [7] have presented a QCA circuits design methodology based on traditional CMOS circuits design flow and a SPICE model.

Ripple carry and carry look ahead adder designs in QCA are presented in [8]. Robust QCA adder designs that exploit proper clocking schemes are proposed in [9]. Probabilistic analysis of molecular quantum-dot cellular adders is presented in [10]. Design of hybrid LFA and RCA using QCA model is presented in [11]. Various concepts such as Robust adders based on QCA, model of QCA circuits using Bayesian networks, Hierarchical probabilistic macro modeling for QCA circuits, Energy dissipation per clock cycle in QCA adder circuits, Cho and Swartz Lander have presented design of a carry flow adder and a multiplier in QCA have been described in previous works. The proposed work begins by developing a QCA-based solution for an adder that is hybrid of ripple carry adder and carry select adder. This hybrid adder is shown to be well-suited to the QCA model. Further, the hybrid adder compares well with existing adders in terms of area of the QCA design (since it incorporates best features of ripple carry

adders). It is also shown that the hybrid adder has a smaller area-delay product than existing adder designs in QCA.

The remainder of this paper is organized as follows. Section III provides the basic notations pertaining to QCA. Section IV presents QCA design and simulation results for the hybrid combination of carry select adder and ripple carry adder. Section V presents the comparison results of the proposed hybrid adder with the previous adders. Section VI deals with the application of hybrid adder in the design of Wallace tree multiplier.

III. BASICS OF QCA

A. QCA Cell

QCA and the QCA cell was first introduced by Prof. C. S. Lent at the University of Notre Dame. QCA information processing is based on the columbic interactions between many identical QCA cells; each constructed using four to six electronic sites coupled through quantum mechanical tunneling barriers. A quantum-dot cellular automaton (QCA) is a square nanostructure of electron wells containing free electrons as shown in Fig. 1. Each QCA cell is a set of four dots positioned at the four corners of a square. Each QCA cell is occupied by two electrons. The electronic sites represent locations that an electron can occupy. In semiconductor implementations, these sites are realized using coupled quantum dots. The cells are designed to contain two mobile electrons which repel each other as a result of their mutual columbic repulsion, and, in the ground state, tend to occupy the diagonal sites of the cell.

Binary information can be encoded in the position of the electrons in the cell. With the placement of the two extra electrons in the four dots and due to the electrostatic repulsion, the two free electrons only can be at two stable positions. These two conditions considered as -1 and +1 polarity or Boolean values 0 and 1 respectively. One of the main discussions of QCA is the intercellular movement of electrons. As it was maintained, the two free electrons of each cell can only be in two stable conditions. The movement of each cell free electrons between its dots is done through the tunneling mechanism.

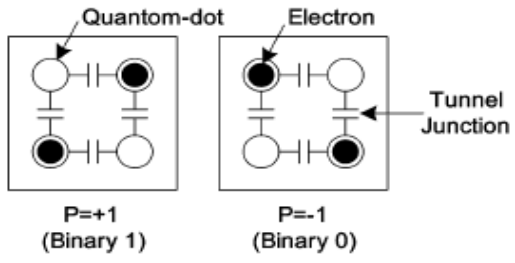

Figure 1: QCA Cells with Electrons and Quantum Dot

B. Clocking in QCA

The movement of electron is done with the help of clocking i.e. to facilitate transfer to a new ground state, another approach based on clocking has been suggested. Clocking (by application of an appropriate voltage to a cell) leads to adjustment of tunneling barriers between quantum dots for transfer of electrons between the dots. Clocking is performed in one of two ways: zone clocking and continuous clocking. In zone clocking, each QCA cell is clocked using a four-phase clocking scheme as shown in Fig. 2. The four phases correspond to *switch*, *hold*, *release* and *relax*. In the switch phase, cells begin unpolarized and with low potential barriers but the barriers are raised during this phase. In the hold phase, the barriers are held high while in the release phase, the barriers are lowered. In the last phase, namely relax, the barriers remain lowered and keep the cells in an unpolarized state. An alternative to zone clocking, called continuous clocking, involves generation of a potential field by a system of submerged electrodes.

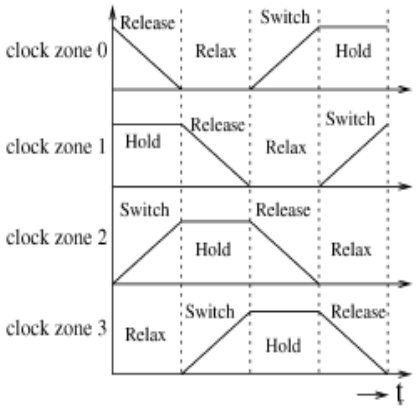

Figure 2: QCA Clock Zones

C. Components of QCA

There are three major components in QCA. With the help of these components the designs of ALU's can be performed. They help in transfer of information from one QCA cell to another cell with the help of polarization effect. A single device is used for the construction of all components of an entire circuit with computational elements and wires. The QCA cell is a basic building block of nanotechnology that can be used to make gates, wires and memories. The basic logic circuits used in this technology are QCA wire, QCA inverter and the Majority Gate (MG), using these all other logical circuits can be designed.

- *QCA Wire*

The concept of a QCA wire is that when the cells are placed in a serial manner then transmission of input appears at the output also. When the output is same as the input then it implies that the wire can be used just for interconnections. In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a $90^{\mathbf{0}}$ QCA wire is shown in Fig.3.Other than the $90^{\mathbf{0}}$ QCA wire, a 45^{0} QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations.

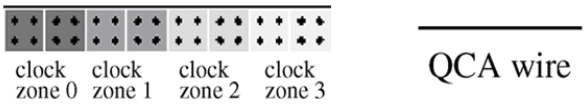

Figure 3: A 900 QCA Wire

- *Inverter*

The next important component of QCA is the inverter. The concept of inverter is that when the cells are placed in a serial manner then it acts as a wire but if it is placed in a parallel manner then it acts as an inverter. A QCA layout of an inverter circuit is shown in Fig. 4. Cells oriented at 45^0 to each other take on opposing polarization. This orientation is employed here to create the inverter shown in this fig. 4.

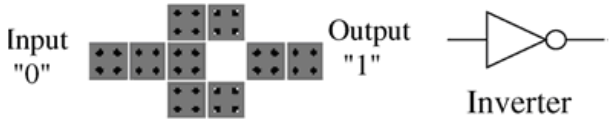

Figure 4: QCA Inverter

- *Majority Gate*

Another important component of QCA is the majority gate. The representation is given in the fig 5. The majority gate performs a three-input logic function. Assuming the inputs is A, B and C, the logic function of the majority gate is given as in (3.1)

$$M(A, B, C) = A.B + B.C + A.C \qquad (3.1)$$

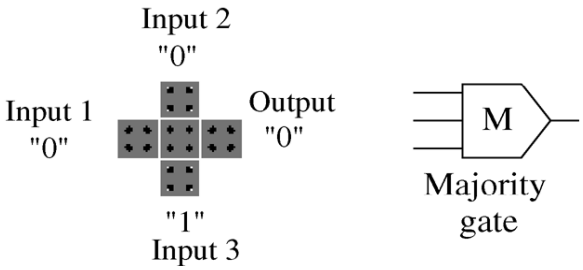

Figure 5: Majority Gate

IV. HYBRID ADDER IN QCA

Hybrid adder circuitry is provided for integrated circuits such as programmable integrated circuits. The hybrid adder may combine the capabilities of multiple adder architectures. Hybrid adders may include carry select and carry ripple adder circuits. The adder circuits may be combined using a carry look-ahead architecture. Adder functionality may be implemented using the resources of logic regions on the programmable integrated circuits. Each logic region may include combinatorial logic such as look-up table logic and register circuitry. The hybrid adder circuitry may receive input words to be added from the combinatorial circuitry and may produce corresponding arithmetic sum output signals to the register circuitry.

Hybrid adder circuitry in accordance with embodiments of the present invention may be part of any suitable integrated circuit. For example, the hybrid adder circuitry of the present invention may be implemented on programmable logic device integrated circuits. If desired, the hybrid adder circuitry may be implemented on programmable integrated circuits that are not traditionally referred to as programmable logic devices such as microprocessors, digital signal processors, application specific integrated circuits, or other integrated circuits with programmable circuitry.

A. Need for Hybrid Adder

While the other adders support parallelism, the requirement of majority gates which contributes to the overall area is quite high. The large number of majority gates has an indirect effect on the wire (delay and amount). It is therefore of interest to explore ways of reducing the area. It is known that ripple carry adders are simple and have low area requirement and carry select adder are fastest adder among other adders. So this fact is taken advantage of in this proposed design of hybrid adder.

B. Hybrid of RCA and CSLA

Generally, a Carry-Select adder (CSLA) is a particular way to implement an adder, which is a logic element that computes the (n + 1) bit sum of two n-bit numbers. The carry-select adder is simple but rather fast, having a gate level depth of $O(\sqrt{n})$. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\lfloor \sqrt{n} \rfloor$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

A ripple carry adder allows adding two k-bit numbers. Half adders and full adders are used in RCA to process the propagation of sum and carry. The layout of a ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. Concatenating the N full adders forms N bit Ripple carry adder. In this carry out of previous full adder becomes the input carry for the next full adder. As carry ripples from one full adder to the other, it traverses longest critical path and

exhibits worst case delay. But this disadvantage is overcome by combining the RCA with CSLA. The hybrid combination of proposed adder is shown in fig. 6.

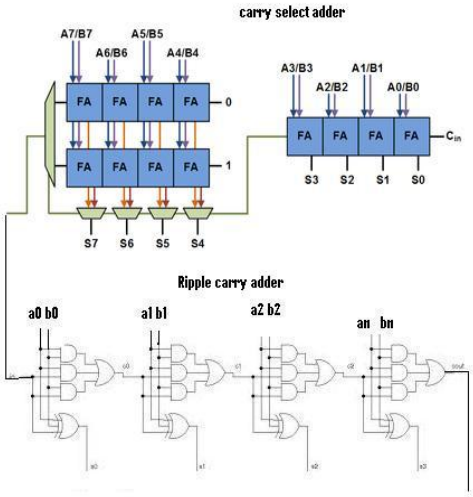

Figure 6: Proposed Hybrid Combination of RCA and CSLA

V. Comparison Results of Proposed Adder with Previous Adder

The results produced by the proposed hybrid adder are compared with the previous adder which is a combination of LFA- Ladner Ficsher adder and RCA- Ripple Carry adder. The comparison result shows that the area-delay product is reduced when LFA is replaced by CSLA in the proposed hybrid adder. Tables 1& 2 shows the area-delay product of previous and proposed adders respectively.

Table i. Area-Delay of Previous Hybrid Adder (LFA & RCA)

NO. OF BITS CONSIDERED	NO. OF LUT's USED	NO. OF BONDED IOB's	DELAY PRODUCED (ns)
16	51	48	15.093
32	76	97	42.485

Table ii. Area-Delay of proposed Hybrid Adder: (CSLA & RCA)

NO. OF BITS CONSIDERED	NO. OF LUT's USED	NO. OF BONDED IOB's	DELAY PRODUCED (ns)
16	16	26	14.846
32	63	89	33.621

VI. Application of Hybrid Adder

Hybrid adders are not only used in area delay reduction but also may be used in application in which multipliers may find the use of this hybrid adder in the fast production of partial products during multiplication process. As a result, the speed can be enhanced; the area–delay product is also decreased.

A. *Wallace Tree Multiplication*

Wallace tree is known for their optimal computation time, when adding multiple operands to two outputs using carry-save adders. The Wallace tree guarantees the lowest overall delay but requires the largest number of wiring tracks i.e. vertical feed throughs between adjacent bit-slices. The number of wiring tracks is a measure of wiring complexity. Fig 7 shows an Wallace tree, where CSLA indicates a carry-select adder having three multi-bit inputs and two multi-bit outputs.

The need for choosing Wallace tree multiplier in this proposed work is that it is the advance type of multiplier that is used among the multipliers used in VLSI adders. It is fast and robust in its characteristics so to increase this added advantage the outputs of the 16 bit hybrid adder is given to the Wallace tree multiplier hence reducing the area of the multiplier.

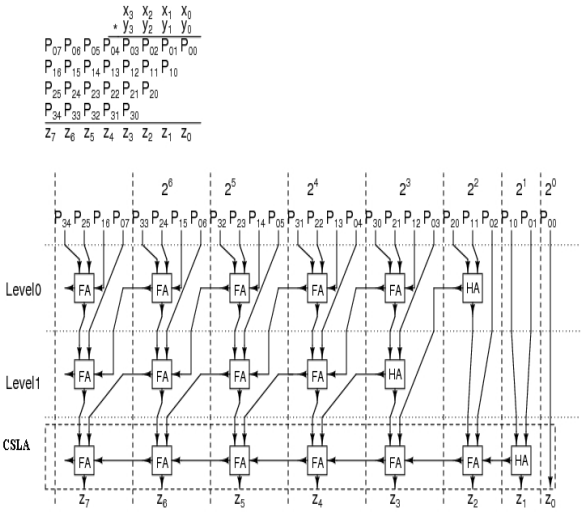

Figure 7: Wallace Tree Multiplication

B. *Application of Hybrid Adder in Wallace Tree Multiplier*

The hybrid adder which is designed using QCA model is used in a Wallace tree multiplier. As a result of implementing the use of hybrid adder in this multiplier the area and delay can be reduced. The application can be implemented by considering the outputs of a 16 bit hybrid adder which is given to a Wallace tree multiplier. This involves the usage of full adders and 16 bit hybrid adder. Here, the usage of half adders is totally avoided and thus decreasing the area involved in the design of the Wallace tree multiplier. With the help of these adders, it is easy to obtain the output which is produced with less area and less delay. The below figure shows the simulation result of Wallace tree multiplier.

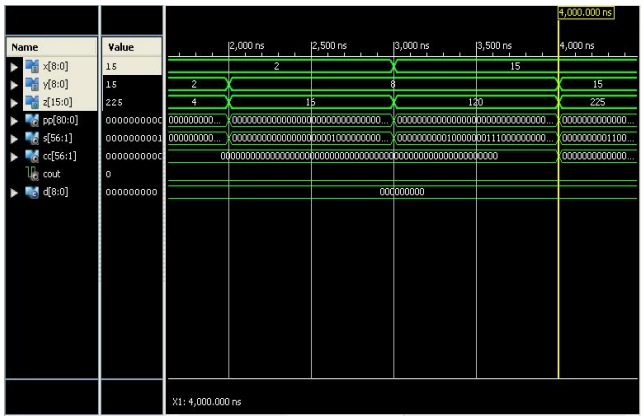

Figure 8: Simulation Result of Wallace Tree Multiplier

VII. CONCLUSION

With the help of QCA technology, the hybrid adder which is the combination of RCA and CSLA is designed and it is applied to the Wallace tree multiplier. This potentially reduces the area-delay product and the comparison result shows that the proposed hybrid adder is well suited for fast computation.

ACKNOWLEDGEMENT

Words are inadequate in offering our thanks to Dr.M.Jagadeeswari, M.E., Ph.D., Professor and Head, Department of VLSI Design and all others who supported us for their encouragement and cooperation in carrying out the project work.

REFERENCES

[1] Bhanja,S. and Sarkar,S. (2006) 'Probabilistic modeling of QCA circuits using Bayesian networks', IEEE Trans. Nanotechnol ., vol. 5, no. 6, pp. 657–670.

[2] Brent,R.P. and Kung,H.T. (1982) 'A regular layout for parallel adders', IEEE Trans. Comput.,vol. C-31, no. 3, pp. 260–264.

[3] Cho,H. and Swartzlander,E.E. (2009) 'Adder and multiplier designs in quantum-dot cellular automata', IEEE Trans. Comput., vol. 58, no.6, pp. 721–727.

[4] Cho,H and Swartzlander,E.E. (2007) 'Adder designs and analyses for quantum-dot cellular automata', IEEE Trans. Nanotechnol., vol. 6, no. 3, pp. 374–383.

[5] Cho,H. and. Swartzlander,E.E. (2006) 'Modular design of conditional sum adders using quantum-dot cellular automata', in Proc. IEEE Conf. Nanotechnol. (IEEE NANO), pp. 363–366.

[6] Dysart,T. and Kogge,M. (2009) 'Analyzing the inherent reliability of moderately sized magnetic and electrostatic QCA circuits via probabilistic transfer matrices', IEEE Trans. Very Large Scale Integr.(VLSI) Syst.,vol. 17, no 4, pp.507-513.

[7] Dysart,T.J. and Kogge,M. (2007) 'Probabilistic analysis of a molecular quantum-dot cellular automata adder', in Proc. IEEE Symp Defect Fault Toler.VLSI Syst., pp. 478–486.

[8] Hanninen,I. and Takala,J. (2007) 'Robust adders based on quantum-dot cellular automata', in proc.IEEE Int. Conf. Appl-Specific Syst.,Arch Processors, pp.391-396.

[9] Huang,J. and Momenzadeh,M. (2007) 'An overview of nanoscale devices and circuits', IEEE Des. Test Comput., vol. 24, no.4, pp. 304

[10] Han,T. and Carlson,D.A. (1987) 'Fast area-efficient VLSI adders,' in Proc 8th IEEE Symp, Comput. Arith., pp. 49–56.

[11] Vikramkumar Pudi and Sridharan, K. (2011) 'Efficient Design of a Hybrid Adder in Quantum-Dot Cellular Automata', IEEE Trans. Very Large Scale Integr.(VLSI) Syst.,vol. 19, no 9, pp.1535-1547.